Type : Question

Branch : ECE

Sem : 3rd Semester

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Unit – I Boolean algebra and Logic Gates

Part A

1. Find the hexadecimal equivalent of the decimal number 256

2. Find the octal equivalent of the decimal number 64

3. What is meant by weighted and non-weighted coding?

4. Convert A3BH and 2F3H into binary and octal respectively

5. Find the decimal equivalent of (123)9

6. Find the octal equivalent of the hexadecimal number AB.CD

7. Encode the ten decimal digits in the 2 out of 5 code

8. Show that the Excess – 3 code is self –complementing

9. Find the hexadecimal equivalent of the octal number 153.4

10. Find the decimal equivalent of (346)7

11. A hexadecimal counter capable of counting up to at least (10,000)10 is to be constructed.

What is the minimum number of hexadecimal digits that the counter must have?

12. Convert the decimal number 214 to hexadecimal

13. Convert 231.3 4 to base 7

14. Give an example of a switching function that contains only cyclic prime implicant

15. Give an example of a switching function that for which the MSP from is not unique.

16. Express x+yz as the sum of minterms

17. What is prime implicant?

18. Find the value of X = A B C (A+D) if A=0; B=1; C=1 and D=1

19. What are ‘minterms’ and ‘maxterms’?

20. State and prove Demorgan’s theorem

21. Find the complement of x+yz

22. Define the following : minterm and term

23. State and prove Consensus theorem

24. What theorem is used when two terms in adjacent squares of K map are combined?

25. How will you use a 4 input NAND gate as a 2 input NAND gate?

26. How will you use a 4 input NOR gate as a 2 input NOR gate?

27. Show that the NAND connection is not associative

28. What happens when all the gates is a two level AND-OR gate network are replaced by NOR gates?

29. What is meant by multilevel gates networks?

30. Show that the NAND gate is a universal building block

31. Show that a positive logic NAND gate is the same as a negative logic NOT gate

32. Distinguish between positive logic and negative logic

33. Implement AND gate and OR gate using NAND gate

34. What is the exact number of bytes in a system that contains (a) 32K byte, (b) 64M

bytes, and (c) 6.4G byte?

35. List the truth table of the function:

F = x y + x y’ + y ’z

Part B

1. (a) Explain how you will construct an (n+1) bit Gray code from an n bit

Gray code

(b) Show that the Excess – 3 code is self -complementing

2. (a) Prove that (x1+x2).(x1'. x3'+x3) (x2' + x1.x3) =x1'x2

(b) Simplify using K-map to obtain a minimum POS expression: (A' + B'+C+D) (A+B'+C+D) (A+B+C+D') (A+B+C'+D') (A'+B+C'+D') (A+B+C'+D)

3. Reduce the following equation using Quine McClucky method of minimization F (A,B,C,D) = _m(0,1,3,4,5,7,10,13,14,15)

4. (a) State and Prove idempotent laws of Boolean algebra.

(b) using a K-Map ,Find the MSP from of F= _(0,4,8,12,3,7,11,15) +_d(5)

5 (a) With the help of a suitable example ,explain the meaning of an redundant prime i Zimplicant

(b) Using a K-Map, Find the MSP form of F= _ (0-3, 12-15) + _d (7, 11)

6 (a) Simplify the following using the Quine – McClusky minimization technique D = f(a,b,c,d) = _ (0,1,2,3,6,7,8,9,14,15).Does Quine –McClusky take care of don't care conditions? In the above problem, will you consider any don't care conditions? Justify your answer

(b) List also the prime implicants and essential prime implicants for the above case

7 (a) Determine the MSP and MPS focus of F= _ (0, 2, 6, 8, 10, 12, 14, 15)

(b) State and Prove Demorgan's theorem

8 Determine the MSP form of the Switching function

F = _ (0,1,4,5,6,11,14,15,16,17,20- 22,30,32,33,36,37,48,49,52,53,56,63)

9. (a) Determine the MSP form of the Switching function

F(a,b,c,d) =_(0,2,4,6,8) + _d(10,11,12,13,14,15)

(b) Find the Minterm expansion of f(a,b,c,d) = a'(b'+d) + acd'

10 Simplify the following Boolean function by using the Tabulation Method

F= _ (0, 1, 2, 8, 10, 11, 14, 15)

11 State and Prove the postulates of Boolean algebra

12 (a) Find a Min SOP and Min POS for f = b'c'd + bcd + acd' + a'b'c + a'bc'd

13 Find an expression for the following function usingQuine McCluscky method

F= _ (0, 2, 3,5,7,9,11,13,14,16,18,24,26,28,30)

14 State and Prove the theorems of Boolean algebra with illustration

15 Find the MSP representation for

F(A,B,C,D,E) = _m(1,4,6,10,20,22,24,26) + _d (0,11,16,27) using K-Map method

Draw the circuit of the minimal expression using only NAND gates

16 (a) Show that if all the gates in a two – level AND-OR gate networks are replaced by

NAND gates the output function does not change

(b) Why does a good logic designer minimize the use of NOT gates?

17 Simplify the Boolean function F(A,B,C,D) = _ m (1,3,7,11,15) + _d (0,2,5) .if don't

care conditions are not taken care, What is the simplified Boolean function .What are your comments on it? Implement both circuits

18 (a) Show that if all the gate in a two – level OR-AND gate network are replaced by

NOR

gate, the output function does not change.

(b) Implement Y = (A+C) (A+D') (A+B+C') using NOR gates only

19 (a) F3 = f(a,b,c,d) = _ (2,4,5,6) F2 = f(a,b,c,d) = _ (2,3,,6,7)

F1 = f(a,b,c,d) = _ (2,5,6,7) .Implement the above Boolean functions

(i) When each is treated separately and

(ii)When sharing common term

(b) Convert a NOR with an equivalent AND gate

20 Implement the Switching function whose octal designation is 274 using NAND

gates only

21 Implement the Switching function whose octal designation is 274 using NOR gates only

22 (a) Show that the NAND operation is not distributive over the AND operation

(b) Find a network of AND and OR gate to realize f(a,b,c,d) = _ m (1,5,6,10,13,14)

23 What is the advantages of using tabulation method? Determine the prime implicants of the following function using tabulation method

F(W,X,Y,Z) = _(1,4,6,7,8,9,10,11,15)

23 (a) Explain about common postulates used to formulates various algebraic structures

(b) Given the following Boolean function F= A"C + A'B + AB'C + BC

Express it in sum of minterms & Find the minimal SOP expression

Unit – II Combinational Logic

Part A

1. How will you build a full adder using 2 half adders and an OR gate?

2. Implement the switching function Y= BC' + A'B + D

3. Draw 4 bit binary parallel adder

4. Write down the truth table of a full adder

5. Write down the truth table of a full sub tractor

6. Write down the truth table of a half sub tractor

7. Find the syntax errors in the following declarations (note that names for primitive gates are optional):

module Exmp1-3(A, B, C, D, F)

inputs A,B,C, and g1(A,B,D); not (D,B,A); OR (F,B,C);

endmodule ;

8. Draw the logic diagram of the digital circuit specified by module circt (A,B,C,D,F);

input A,B,C,D;

output F;

wire w,x,y,z,a,d; and (x,B,C,d); and y,a,C);

and (w,z,B);

or (z,y,A); or (F,x,w); not (a,A); not (d,D); endmodule

9. Define Combinational circuits

10. Define Half and Full adder

11. Give the four elementary operations for addition and subtraction

12. Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the

binary value of the inputs is less than 3.The output is 0 otherwise

13. Define HDL

14. What do you mean by carry propagation delay?

15. What is code converter?

16. Give short notes on Logic simulation and Logic synthesis

17. What do you mean by functional and timing simulation?

18. What do you mean by test bench?

19. Give short notes on simulation versus synthesis

20. Define half sub tractor and full sub tractor

Part B

1 Design a 4 bit magnitude comparator to compare two 4 bit number

2 Construct a combinational circuit to convert given binary coded decimal number into an

Excess 3 code for example when the input to the gate is 0110 then the circuit should generate output as 1001

3 Design a combinational logic circuit whose outputs are F1 = a'bc + ab'c and

F2 = a' + b'c + bc'

4 (a) Draw the logic diagram of a *-bit 7483 adder

(b) Using a single 7483, Draw the logic diagram of a 4 bit adder/sub tractor

5 (a) Draw a diode ROM, which translates from BCD 8421 to Excess 3 code

(b) Distinguish between Boolean addition and Binary addition

6 Realize a BCD to Excess 3 code conversion circuit starting from its truth table

7 (a) Design a full sub tractor

(b) How to it differ from a full sub tractor

8 Design a combinational circuit which accepts 3 bit binary number and converts its

equivalent excess 3 codes

9 Derive the simplest possible expression for driving segment "a" through 'g' in an

8421

BCD to seven segment decoder for decimal digits 0 through 9 .Output should be active high (Decimal 6 should be displayed as 6 and decimal 9 as 9)

10 Write the HDL description of the circuit specified by the following Boolean function

(i) Y= (A+B+C) (A'+B'+C')

(ii) F= (AB' + A'B) (CD'+C'D) (iii) Z = ABC + AB' + A(D+B) (iv) T= [(A+B} {B'+C'+D')]

11 Design 16 bit adder using 4 7483 ICs

Unit – III Design with MSI Devices

Part A

1. What is a decoder and obtain the relation between the number of inputs 'n' and

outputs

'm' of a decoder?

2. Distinguish between a decoder and a demultiplexer

3. Using a single IC 7485 ; draw the logic diagram of a 4 bit comparator

4. what is decoder

5. What do you mean by encoder?

6. Write the short notes on priority encoder

7. What is multiplexer? Draw the logic diagram of8 to 1 line multiplexer

8. What do you mean by comparator?

9. Write the HDL description of the circuit specified by the following Boolean function

X=AB+ACD+BC'

10. How does ROM retain information?

11. Distinguish between PAL and PLA

12. Give the classification of memory

13. What is refreshing? How it is done?

14. What is Hamming code?

15. Write a short notes on memory decoding

16. List the basic types of programmable logic devices

17. What is PAL? How it differ from PROM and PLA?

18. Write a short notes on – PROM,EPROM,EEPROM

19. How many parity bits are required to form Hamming code if massage bits are 6?

20. How to find the location of parity bits in the Hamming code?

21. Generate the even parity Hamming codes for the following binary data

1101, 1001

22. A seven bit Hamming code is received as 11111101. What is the correct code?

23. Compare static RAMs and dynamic RAMs

24. Define Priority encoder

25. Define PLDs

Part B

1. Implement the switching function F= _(0,1,3,4,7) using a 4 input MUX and explain

2. Explain how will build a 64 input MUX using nine 8 input MUXs

3. State the advantages of complex MSI devices over SSI gates

4. Implement the switching function F(A,B,C) = _ (,2,4,5) using the DEMUX 74156

5. Implement the switching function F= _(0,1,3,4,12,14,15) using an 8 input MUX

6. Explain how will build a 16 input MUX using only 4 input MUXs

7. Explain the operation of 4 to 10 line decoder with necessary logic diagram

8. Draw a neat sketch showing implementation of Z1 = ab'd'e + a'b'c'e' + bc + de , Z2 = a'c'e, Z3 = bc +de+c'd'e'+bd and Z4 = a'c'e +ce using a 5*8*4 PLA

9. Implement the switching functions:

Z1 = ab'd'e + a'b'c'e' + bc + de , Z2 = a'c'e,

Z3 = bc +de+c'd'e'+bd and

Z4 = a'c'e +ce Using a 5*8*4 PLA

10 Design a switching circuit that converts a 4 bit binary code into a 4 bit Gray code using

ROM array

11.Design a combinational circuit using a ROM ,that accepts a 3- bit number and generates an output binary number equal to the square of the given input number

Unit – IV Synchronous Sequential Logic

Part A

1. Derive the characteristic equation of a D flip flop

2. Distinguish between combinational and sequential logic circuits

3. What are the various types of triggering of flip-flops?

4. Derive the characteristic equation of a T flip flop

5. Derive the characteristic equation of a SR flip flop

6. What is race round condition? How it is avoided?

7. List the functions of asynchronous inputs

8. Define Master slave flip flop

9. Draw the state diagram of 'T' FF, 'D' FF

10. Define Counter

11. What is the primary disadvantage of an asynchronous counter?

12. How synchronous counters differ from asynchronous counters?

13. Write a short note on counter applications

14. Compare Moore and Mealy models

15. When is a counter said to suffer from lock out?

16. What is the minimum number of flip flops needed to build a counter of modulus z

8?

17. State the relative merits of series and parallel counters

18. What are Mealy and Moore machines?

19. When is a counter said to suffer from lockout?

20. What is the difference between a Mealy machine and a Moore Machines?

21. Distinguish between synchronous and asynchronous sequential logic circuits

22. Derive the characteristic equation of a JK flip flop

23. How will you convert a JK flip flop into a D flip flop

24. What is mean by the term 'edge triggered'?

25. What are the principle differences between synchronous and asynchronous networks

26. What is lockout? How it is avoided?

27. What is the pulse mode operation of asynchronous sequential logic circuits not very popular?

28. What are the advantages of shift registers?

29. What are the applications of a shift register?

30. How many flip –flops are needed to build an 8 bit shift register?

31. A shift register comprises of JK flip-flops. How will you complement of the counters of the register

32. List the basic types of shift registers in terms of data movement.

33. Write a short notes on PRBS generator

34. Give the HDL dataflow description for T flip - flop

35. Give the HDL dataflow description for JK flip – flop

Part B

1 Draw the state diagram and characteristics equation of T FF, D FF and JK FF

2 (a) What is race around condition? How is it avoided?

(b) Draw the schematic diagram of Master slave JK FF and input and output waveforms.Discuss how it prevents race around condition

3 Explain the operation of JK and clocked JK flip-flops with suitable diagrams

4 Draw the state diagram of a JK flip- flop and D flip – flop

5 Design and explain the working of a synchronous mod – 3 counter

6 Design and explain the working of a synchronous mod – 7 counter

7 Design a synchronous counter with states 0,1, 2,3,0,1 ……. Using JK FF

8 Using SR flip flops, design a parallel counter which counts in the sequence

000,111,101,110,001,010,000 …….

9 Using JK flip flops, design a parallel counter which counts in the sequence

000,111,101,110,001,010,000 …….

10 (a) Discuss a decade counter and its working principle

(b) Draw as asynchronous 4 bit up-down counter and explain its working

11 (a) How is the design of combinational and sequential logic circuits possible with

PLA?

(b) Mention the two models in a sequential circuit and distinguish between them

12 Design a modulo 5 synchronous counter using JK FF and implement it. Construct its timing diagram

12 A sequential machine has one input line where 0's and 1's are being incident. The machine has to produce a output of 1 only when exactly two 0's are followed by a '1' or exactly two 1's are followed by a '0'.Using any state assignment and JK flipflop,synthesize the machine

13 Using D flip –flop ,design a synchronous counter which counts in the sequence

000, 001, 010, 011, 100, 1001,110,111,000

15 Using JK flip-flops, design a synchronous sequential circuit having one and one output. the output of the circuit is a 1 whenever three consecutive 1's are observed. Otherwise the output is zero

14 Design a binary counter using T flip – flops to count in the following sequences: (i) 000,001,010,011,100,101,110,111,000

(ii) 000,100,111,010,011,000

15 (a) Design a synchronous binary counter using T flip – flops

(b) Derive the state table of a serial binary adder

17. Design a 3 bit binary Up-Down counter

18. (i) Summarize the design procedure for synchronous sequential circuit

(ii) Reduce the following state diagram

Unit – V Asynchronous Sequential Logic

Part A

1. Distinguish between fundamental mode and pulse mode operation of asynchronous

sequential circuits

2. What is meant by Race?

3. What is meant by critical race?

0/0 a

b c d

e

g f

0/0

0/0

1/1

1/1

0/0

1/1

1/1

0/0

1/0

0/0

1/

0

4. What is meant by race condition in digital circuit?

5. Define the critical rate and non critical rate

6. What are races and cycles?

7. What is the significance of state assignment?

8. What are the steps for the analysis of asynchronous sequential circuit?

9. What are the steps for the design of asynchronous sequential circuit?

10. Write short notes on (a) Shared row state assignment

(b) One hot state assignment

11. What are Hazards?

12. What is a static 1 hazard?

13. What is a static 0 hazard?

14. What is dynamic hazard?

15. Define static 1 hazard, static 0 hazards, and dynamic hazard?

16. Describe how to detect and eliminate hazards from an asynchronous network?

17. What is static hazard?

18. List the types of hazards?

19. How to eliminate the hazard?

20. Draw the wave forms showing static 1 hazard?

Part B

1. What is the objective of state assignment in asynchronous circuit? Give hazard –

free

realization for the following Boolean function f(A,B,C,D) = _M(0,2,6,7,8,10,12)

2. Summarize the design procedure for asynchronous sequential circuit a. Discuss on Hazards and races

b. What do you know on hardware descriptive languages?

3. Design an asynchronous sequential circuit with 2 inputs X and Y and with one output Z

Wherever Y is 1, input X is transferred to Z .When Y is 0; the output does not change for

any change in X.Use SR latch for implementation of the circuit

4. Develop the state diagram and primitive flow table for a logic system that has 2 inputs,x

and y and an output z.And reduce primitive flow table. The behavior of the circuit is stated

as follows. Initially x=y=0. Whenever x=1 and y = 0 then z=1, whenever x = 0 and y = 1 then z = 0.When x=y=0 or x=y=1 no change in z ot remains in the previous state. The logic system has edge triggered inputs with out having a clock .the logic system changes

state on the rising edges of the 2 inputs. Static input values are not to have any effect in

changing the Z output

5. Design an asynchronous sequential circuit with two inputs X and Y and with one output Z.

Whenever Y is 1, input X is transferred to Z.When Y is 0,the output does not change

for

any change in X.

6. Obtain the primitive flow table for an asynchronous circuit that has two inputs x,y and one

output Z. An output z =1 is to occur only during the input state xy = 01 and then if the only if

the input state xy =01 is preceded by the input sequence.

7. A pulse mode asynchronous machine has two inputs. It produces an output whenever two

consecutive pulses occur on one input line only .The output remains at '1' until a pulse

has

occurred on the other input line. Draw the state table for the machine.

8.

(a) How will you minimize the number of rows in the primitive state table of an incompletely

specified sequential machine

(b) State the restrictions on the pulse width in a pulse mode asynchronous sequential machine

9. Construct the state diagram and primitive flow table for an asynchronous network that has

two inputs and one output. The input sequence X1X2 = 00,01,11 causes the output to become 1.The next input change then causes the output to return to 0.No other inputs will

produce a 1 output

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